Logic Emulation in the MegaLUT Age: Moore's Law Beats Rent's Rule

Mike Butts

Synopsys Verification Group, Hillsboro, Oregon

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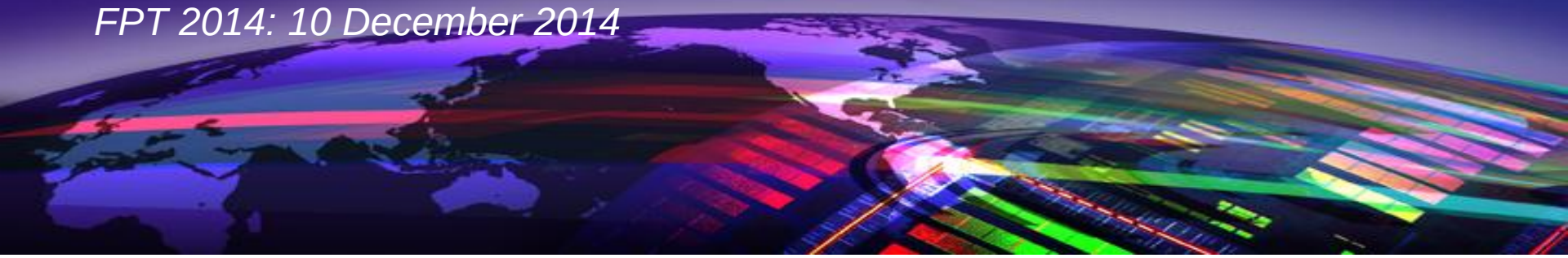
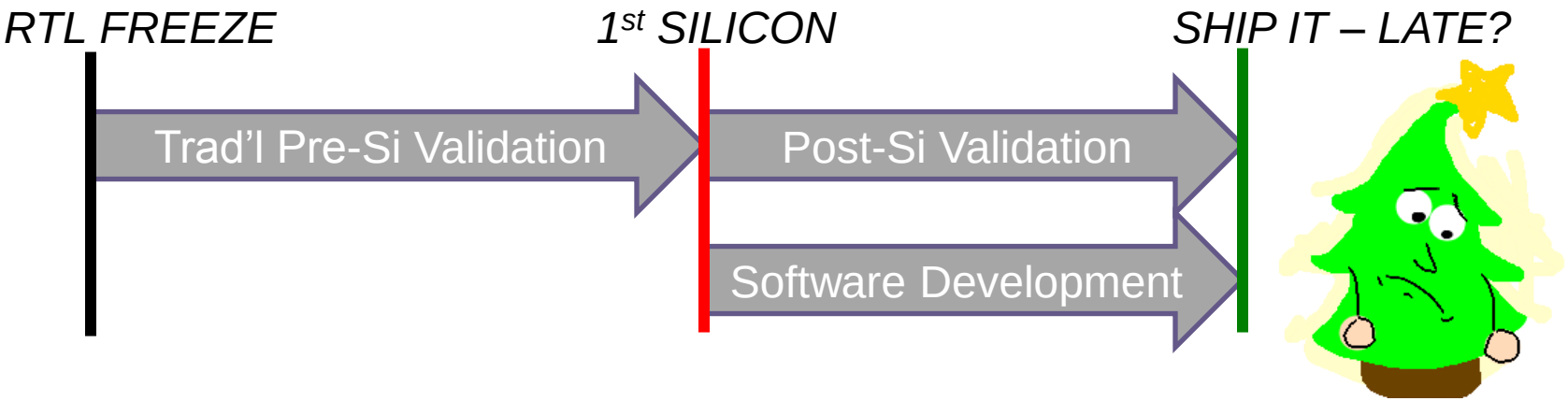


Logic Emulation in the MegaLUT Age: Moore’s Law Beats Rent’s Rule

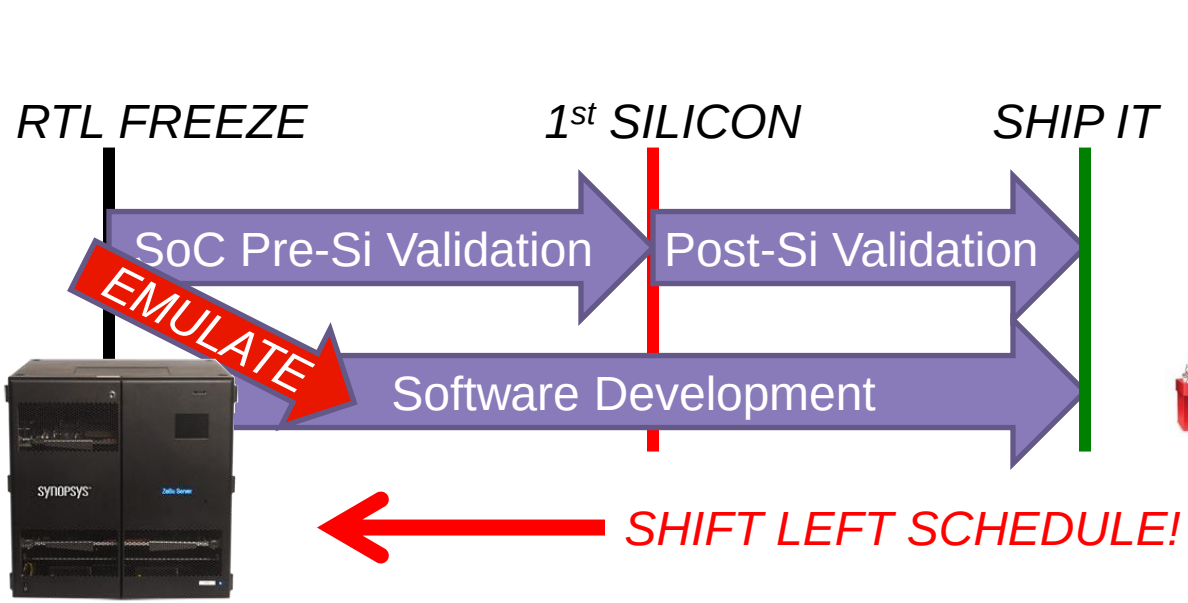
- Logic emulation today
- Rent's Rule and emulation
- Moore's Law and emulation
- Today's Systems on Chips
- Conclusion

Why Tapeouts Use Logic Emulation



- Today's Systems-on-Chip depend critically on software development.
  - Product content is software-huge
  - System-level HW bugs aren't exposed without full software load.
- Starting software development at first silicon is too late!

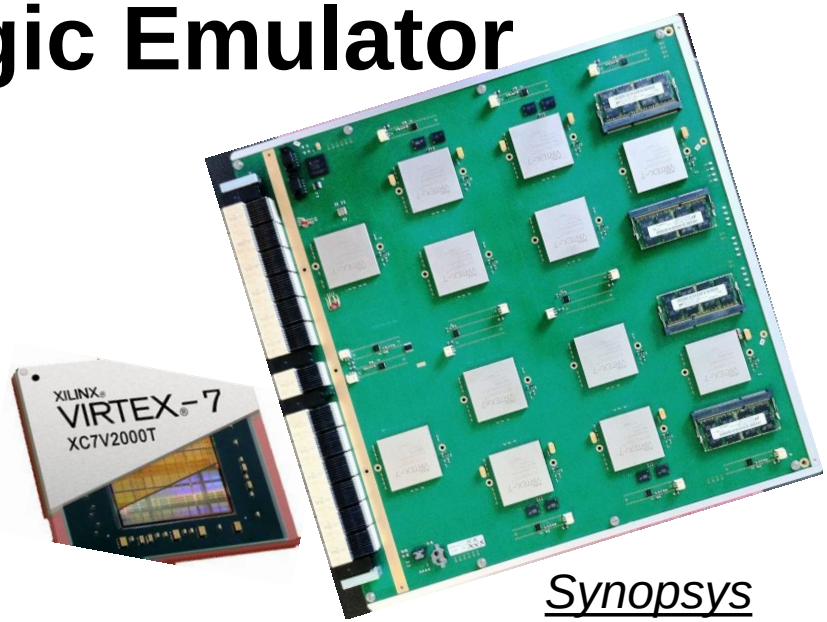
Logic Emulation is Mainstream Today



- Market pressures and system complexity demand a ***shift left*** approach to delivering products.
- Projects require accurate, high-performance models to bring-up/develop/validate software before silicon is ready.
- Emulate at RTL freeze and start software right away!

2014 FPGA-based Logic Emulator

- **Commercial FPGA**
  - Xilinx Virtex-7 2000T
  - 6.6 Million gates, 47M RAM bits
    (Prototypes get more gates by manual effort)
    - 3-D stacked silicon
  - 600 PCB pin pairs @ 1 GHz



Synopsys ZeBu Server 3
60 million gates on one module

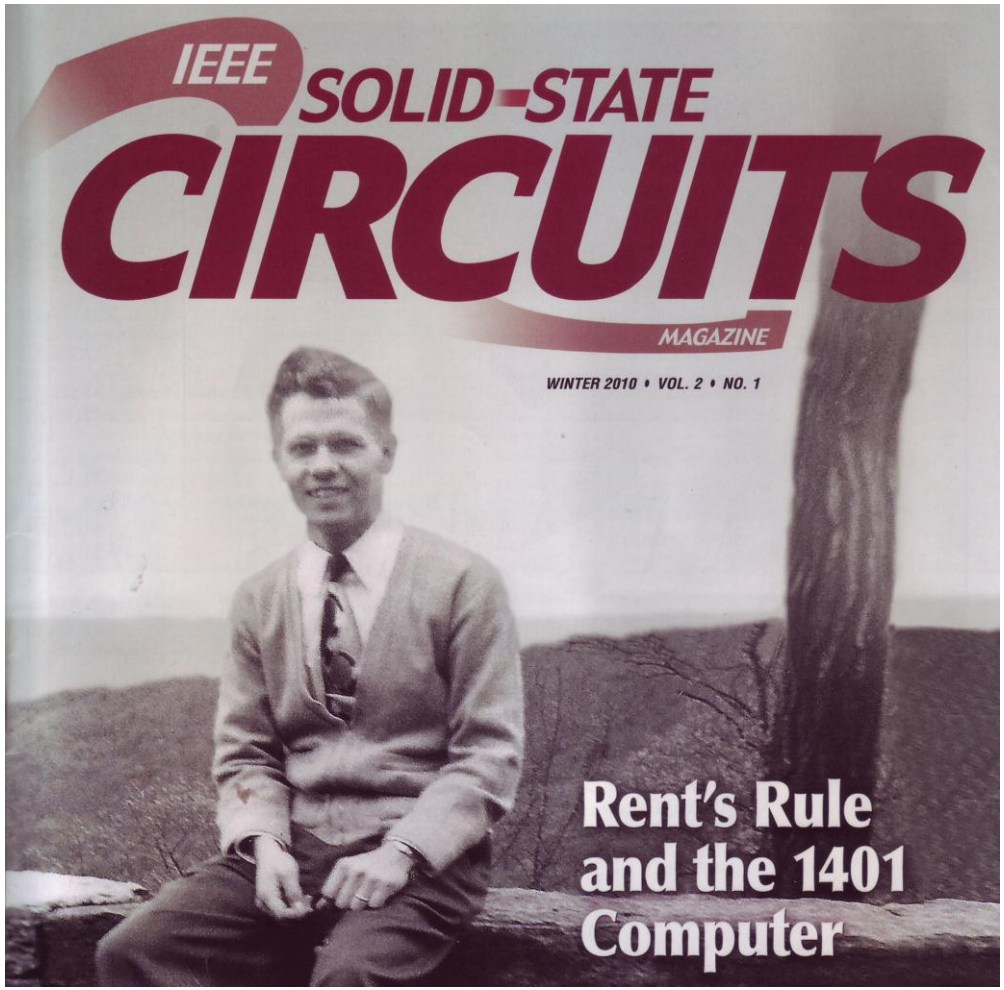
- 300 million gates in 0.2 m^3
  - 60 Mgate module * 5 in a box = 300 Million gates
  - Up to 5MHz emulation speed, less than 3kW.
  - Direct interconnect between FPGAs.
- Scalable to 3 billion gates capacity (600 Virtex-7 2000T FPGAs)
- *Small number of big emulation chips makes this possible.*

History of Rent's Rule

- The problem of how many pins to provide for each partition of a system came up in the IBM 1401 project, 1960.
- Ed Rent found this empirical rule for the relationship between pins per logic block and the number of gates in the block:

$$p = Kg^r$$

where p = pins, g = gates, r is the "Rent exponent", K is the "Rent constant".



History of Rent's Rule

- IBM 1401 used a Standard Modular System (SMS) of logic modules with standard pin counts. How to size? Rent's Rule.
- Rent never published, but in 1971, Landman and Russo did.
  Landman & Russo, On a Pin Versus Block Relationship For Partitions of Logic Graphs, IEEE Trans. Comp., col. C-20, 1971.
- Profound influence on system architecture and CAD/EDA tools.
- Different Rent coefficients apply to different environments.
- Empirical. Theory? Inconclusive.
  - Exponent > 0.5: global connectivity.
  - Constant > 1: net fanout.
- Rent's Rule has been central to logic emulation system architecture.

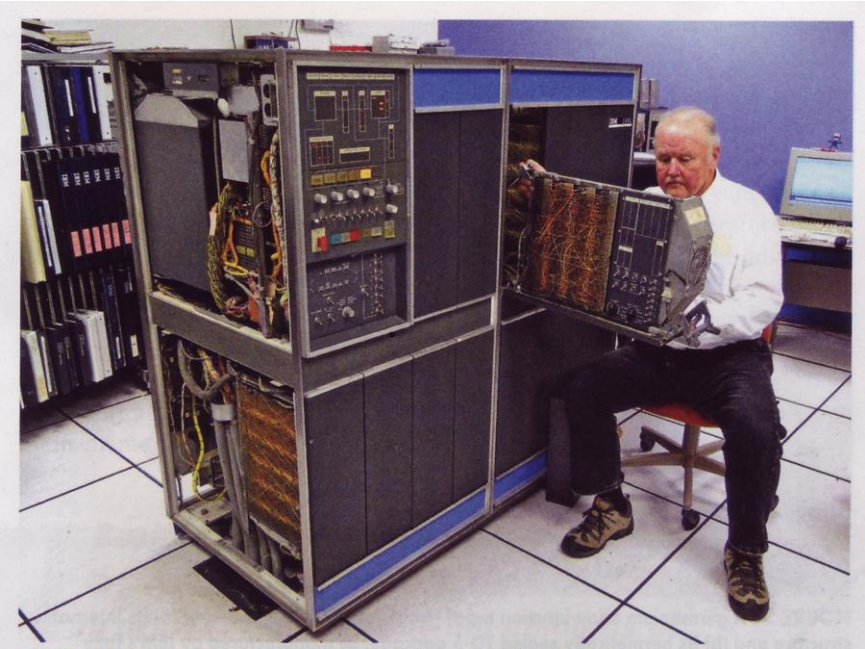


FIGURE 4: Restoration volunteer Ronald Williams and the 1401 processor "main frame" unit, which includes four SMS Cube frames with 24 gates of SMS cards (out of 32 total gate positions); the front panel with indicator lights, buttons, switches, and data paths; 4,000 positions of magnetic core memory; and hard-wired cable bundles to peripherals. The 1401 processor contains about 2,300 SMS cards with 10,600 alloy-junction transistors and 13,200 point-contact diodes. (Photo courtesy of Robert Garner.)

IEEE Solid-State Circuits magazine, winter 2010

Partitioning System Modules Into Small Emulation Chips Cuts Many Nets

- System modules are richly connected inside, with fewer connections to other modules outside.
- **Rent's Rule** applies to modules that get partitioned. It predicts how many internal nets are cut depending on the size of the partition:

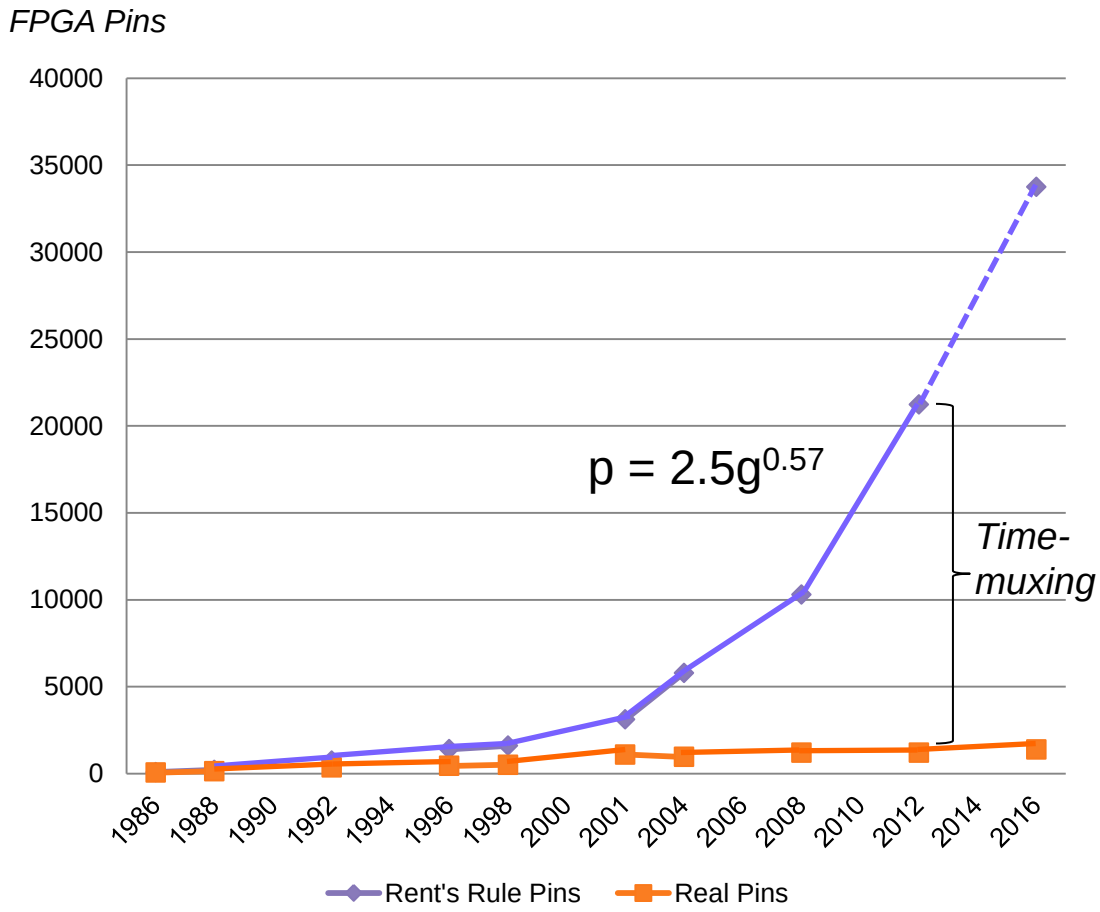
$$Cut\ nets = 2.5 * gates^{0.57}$$

  - 10,000 gate partition cuts 500 nets
  - 100,000 gate partition cuts 1800 nets.
  - 1,000,000 gate partition cuts 6600 nets.

- Partitioning many modules across small chips requires large interconnect HW, which costs speed, power, reliability.

FPGA Logic Emulation and Rent's Rule

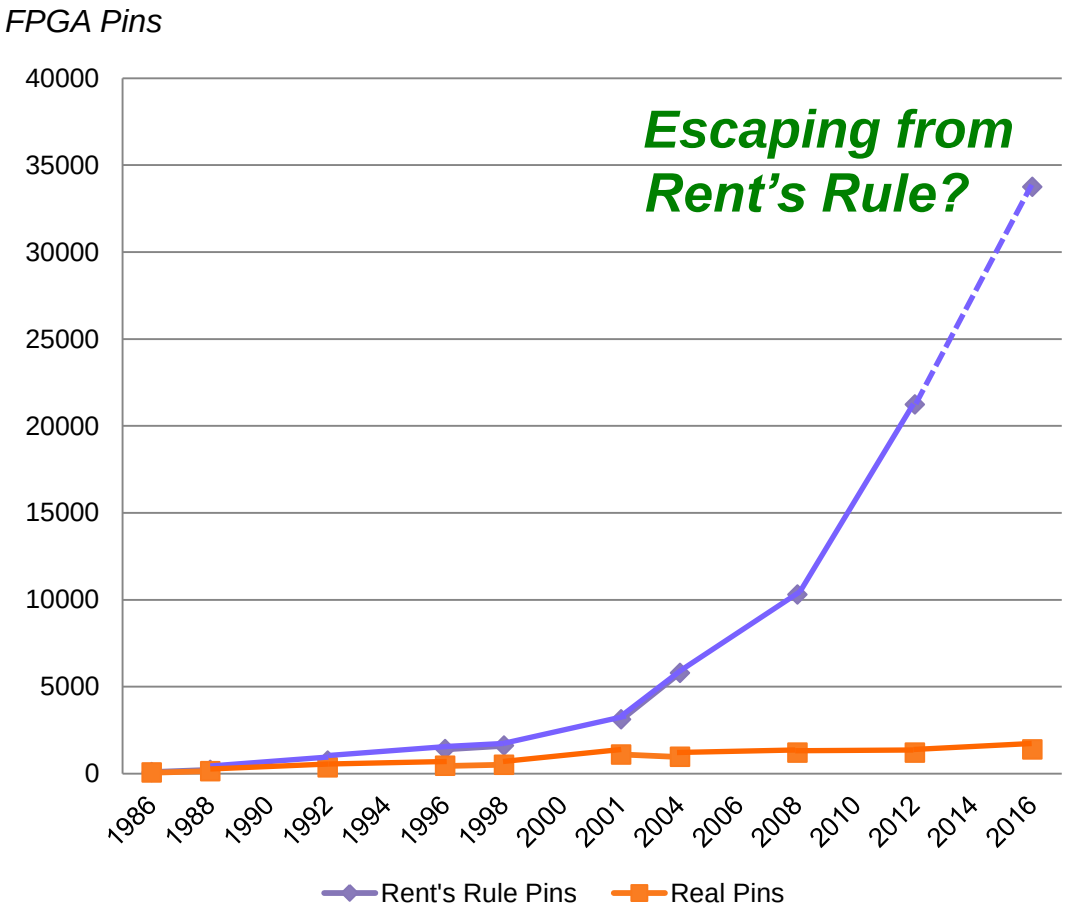
- Rent's Rule pins required have gone up with capacity, much faster than real pins available.
- Gap is filled by time-multiplexing many design nets onto fewer pins.
  - Upwards of 30x per pin, now at GHz rate.
- More cut nets == lower speed



Rent's Rule pins calculated from Xilinx LC capacity.

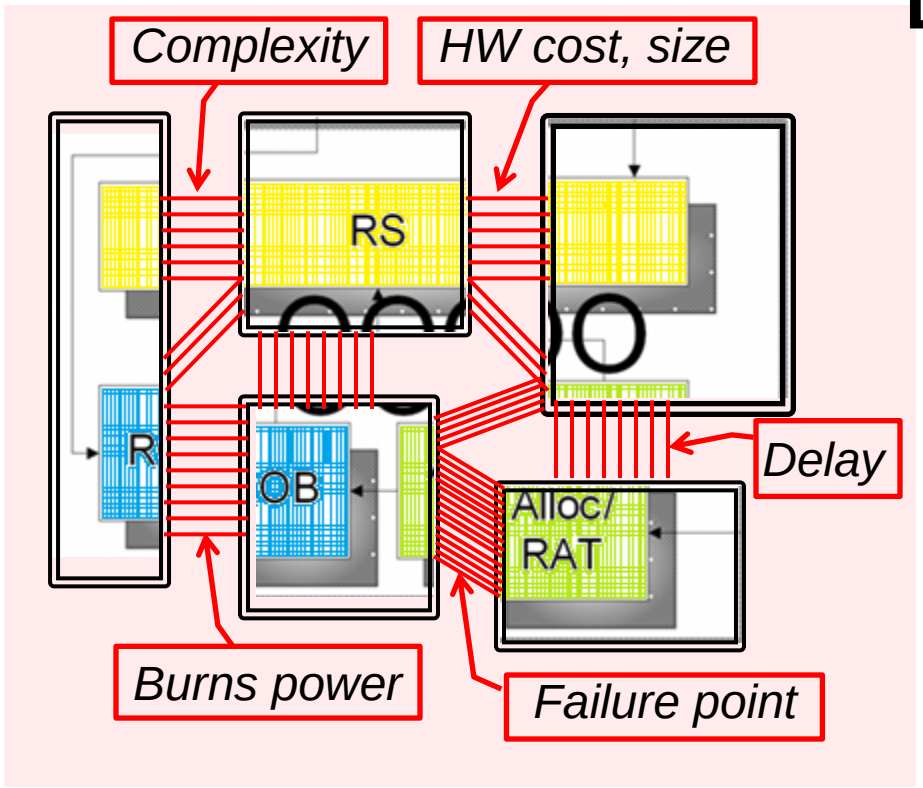
Can Emulation Escape Rent's Rule???

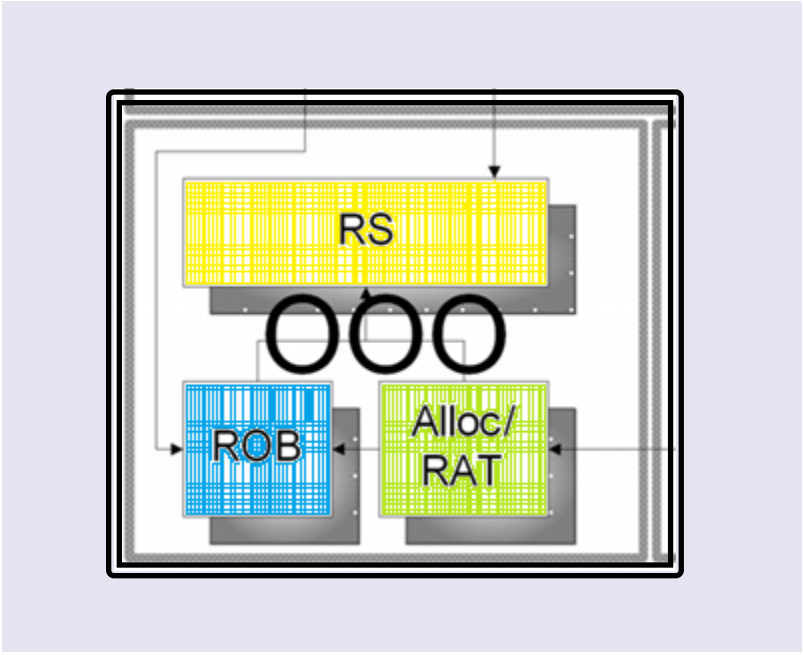
- Rent's Rule applies when each major module gets partitioned into many FPGAs.
- When is that necessary?
  When FPGAs aren't big enough.
- What if FPGAs were big enough to hold entire major modules???



Rent's Rule pins calculated from Xilinx LC capacity.

Small emulation FPGAs need more interconnect, Large FPGAs need less.

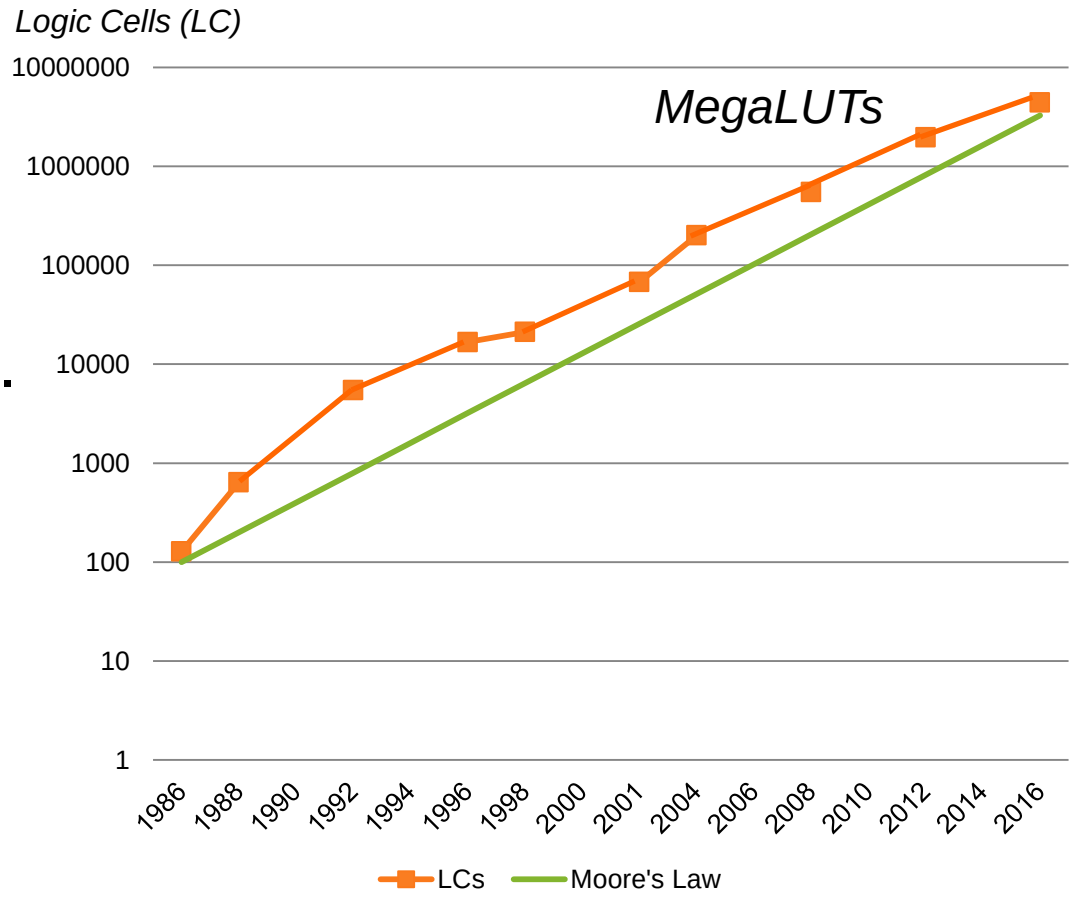




- Module split into 5 small chips
  - Extra cut nets must be interconnected.
  - Interconnect hardware adds delay, power, cost and compile-time complexity, and decreases reliability.
- Module fits in 1 large chip
  - No extra cut nets, just the design's inter-module nets.
  - Faster, cooler, smaller, cheaper, more reliable.

Moore's Law Delivers Ever-Larger FPGAs

- FPGAs have followed Moore's Law density thru their entire history.
- 34,000X in 30 years.
- Why?
  1. Regular, tiled architecture.
  2. Internal routing scaled up according to Rent's Rule.
  3. Useful hard blocks: Memory, Arithmetic



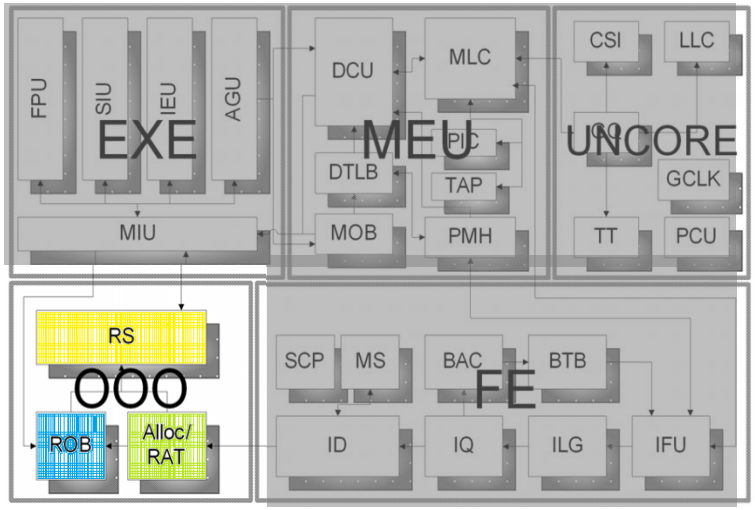
Xilinx LC data, others are similar.
Moore's Law: 2X / 2 years.

Emulation chips should hold entire major modules -- *or else thousands of nets get cut*

- If an entire module fits in an emulation chip, only its system-level nets get cut. There are naturally much fewer of them.
- *In other words, chip capacity outgrows the Rent's Rule range.*
- Example: 3.8 million gate "OOO" module of Intel Nehalem CPU
  - Fits in one 28nm FPGA but must be partitioned with smaller chips.

Emulation Chip	Gates / chip	Chips	Extra cut nets
Virtex7-2000T	**6.6M**	**1**	**zero**
V6-LX550T	1.9M	2	9K
V5-LX330	1.1M	3	10K
Custom Proc.	1M	3	10K
V4-LX160	0.7M	5	13K
Custom FPGA	0.6M	5	12K

"Intel Nehalem Processor Core Made FPGA Synthesizable", ACM FPGA 2010



One big 20nm FPGA can emulate an entire Nehalem CPU with no cut nets

- Components:
  - OOO: 3.8M gates
  - FE: 2.2M gates
  - EXE: 1.5M gates
  - MEU: 1.1M gates
- Total: 8.6M gates

Sizes derived from published prototyping LUT counts: "Intel Nehalem Processor Core Made FPGA Synthesizable", ACM FPGA 2010

FPGA 1

Emulation Chip	Emul Gates	Total Chips	Must Cut Components	Must Cut Module	Extra Cut Nets
UltraScale VU440	**12.5M**	**1**	**No**	**No**	**zero**
Virtex7-2000T	6.6M	2	No	Yes	zero
Custom FPGA	0.6M	15	Yes	Yes	37K

Bigger Chips Beat Rent's Rule 2 Ways

1. When Rent's Rule applies to emulation:
   Bigger chips cut fewer nets. Example 6.6 million gates:
   a) Ten 660,000 gate chips:
      Rent says 660,000 gate partition cuts 5200 nets.
      5200 cut nets * 10 chips = 52,000 total cut nets.
   b) One 6.6 million gate chip:
      Rent says one 6.6M gate partition cuts 19,300 nets.
   10X bigger chip only cuts 37% as many nets.

2. When Rent's Rule doesn't apply to emulation:*
   FPGAs are getting big enough to fit entire major modules.
      Cut nets are system-level buses, which are fewer.
   Rent's Rule only applies to cutting major modules.

** It still applies inside the FPGAs.*

Rent's Rule says Chip Capacity is Everything!!!

- Whether it's a commercial FPGA, a custom FPGA, or a custom processor:

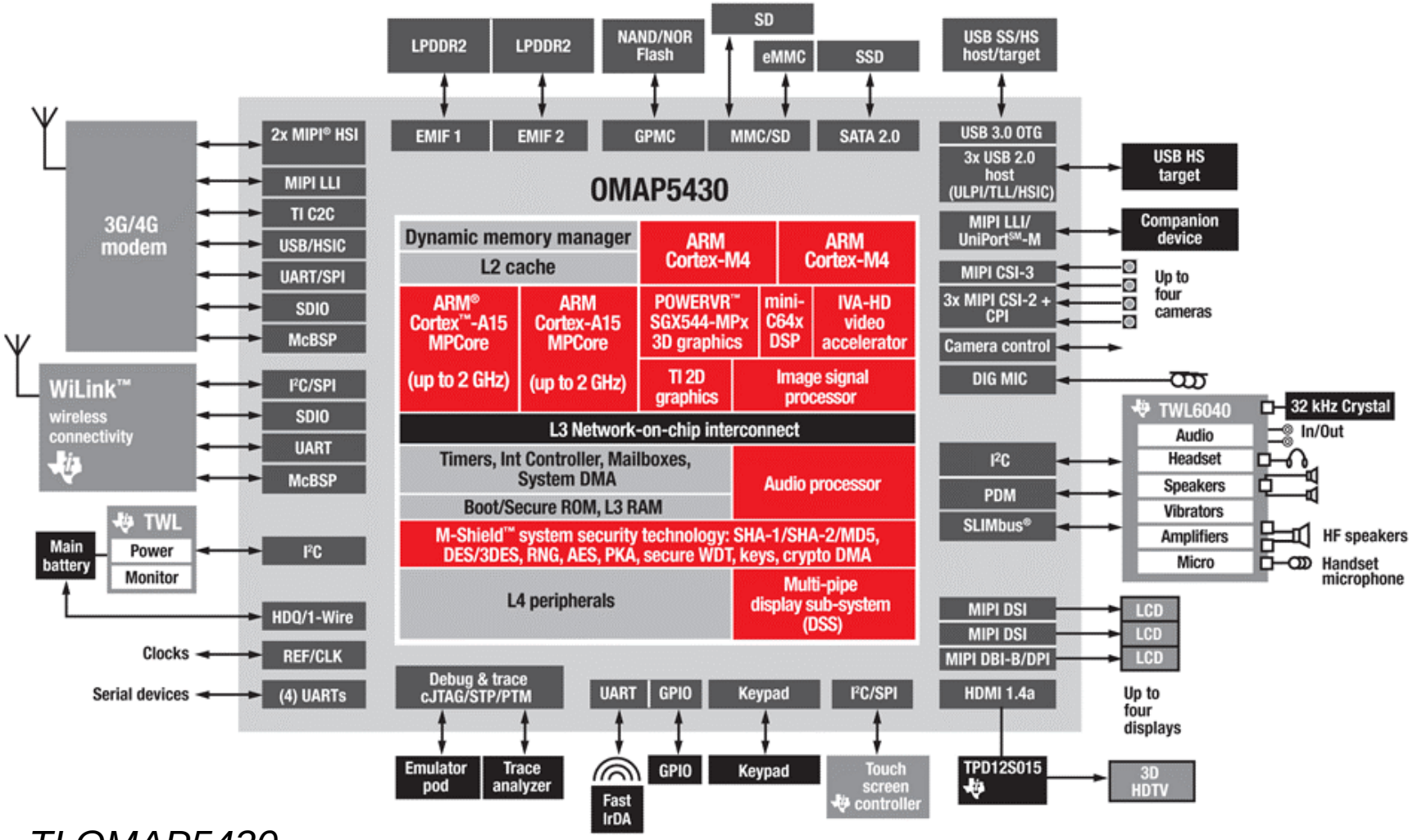
Logic capacity of the emulation chip has a huge impact on emulation speed, cost, size, power, reliability.

- Emulator software partitions the design into small enough fragments to fit in the emulator chips.
- That cuts design nets which must be reconnected.
  - *Cut nets cost speed, cost power, cost space, cost money, and add connections that can fail.*
- **Bigger emulation chips mean fewer cut nets**.

Today's designs have many components

- **System-on-Chip with general and function-specific modules**

Many system modules on one chip

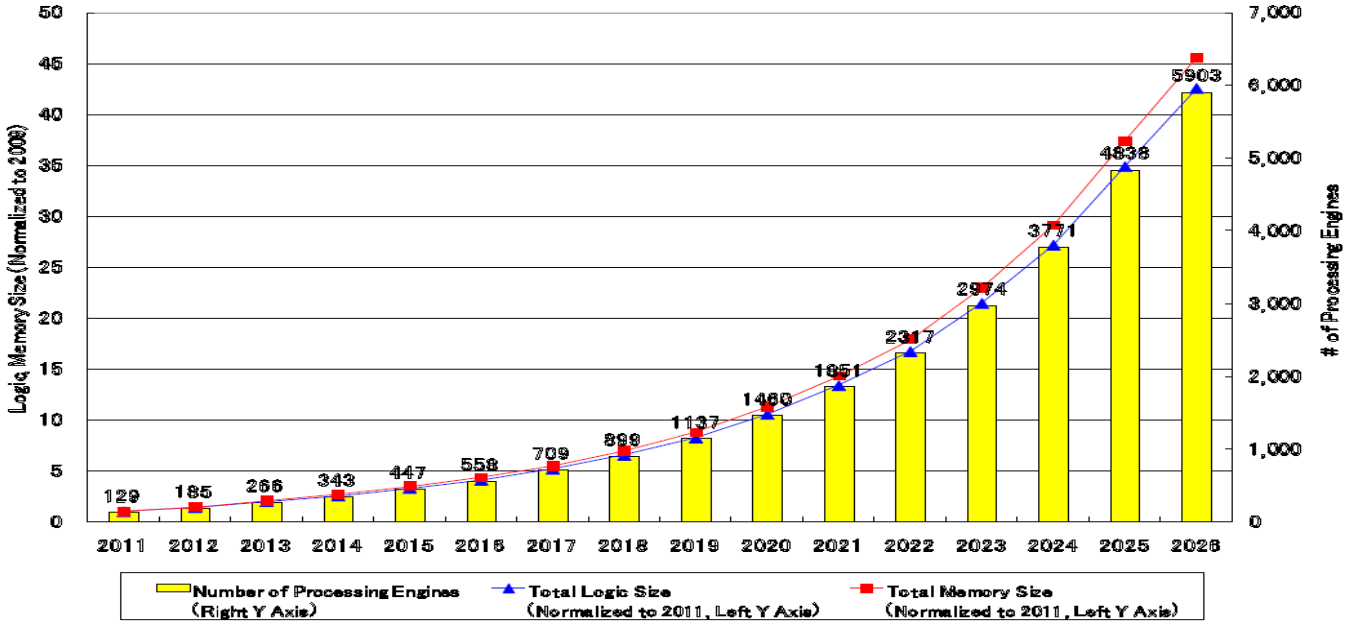


TI OMAP5430 SoC for Tablets

Complexity Trends for Mobile Devices

ITRS 2011 report predicts complexity trend in Consumer Portable SOCs (smart phones, tablets, cameras) as shown in the following chart. The model assumes:

- ***Complexity of main processors will remain constant, but number of processors will grow***
- ***Complexity of peripherals will remain constant***
- ***Complexity of processors customized for specific functions will remain constant, but the number will grow***
- ***Main memory will increase proportional to number of customized processors***



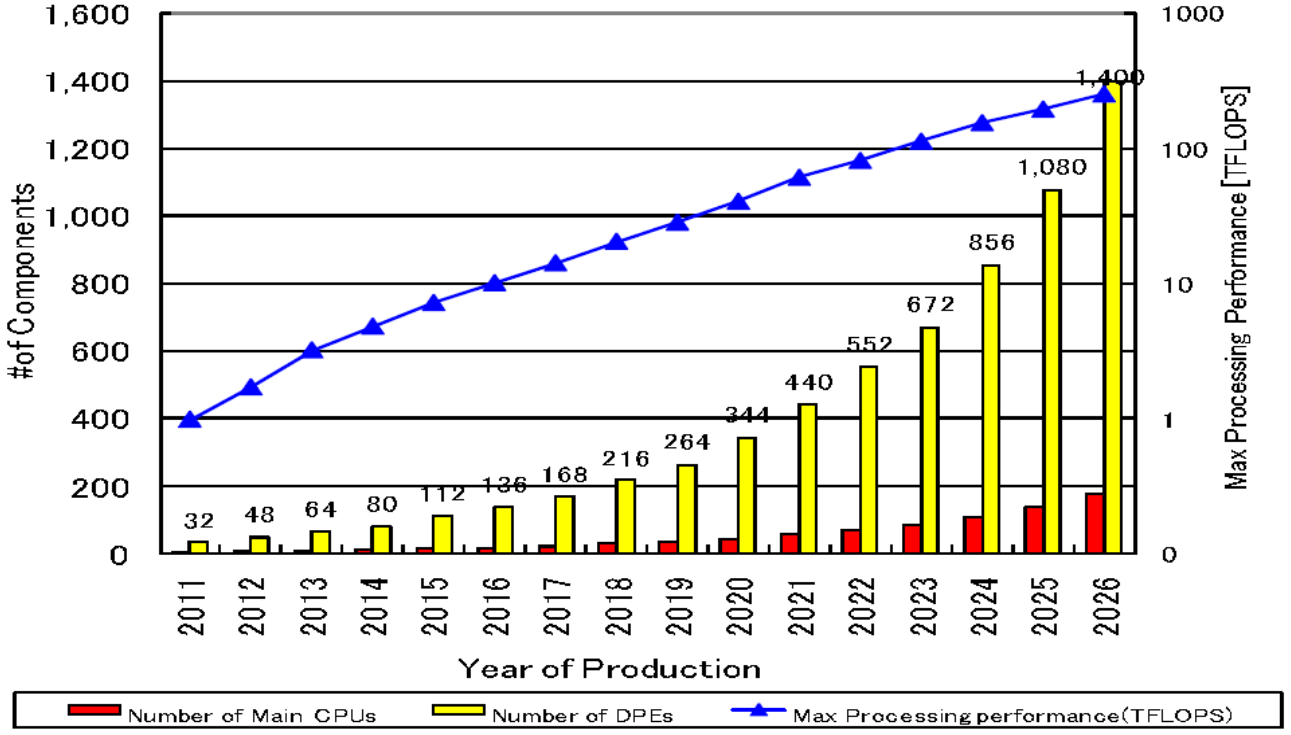
ITRS 2011

Figure SYSD5 SOC Consumer Portable Design Complexity Trends

Complexity Trends for Servers & Games

ITRS 2011 report predicts complexity trend in Consumer Stationary SOCs (non-mobile consumer electronics such as gaming consoles) as shown in the following chart. The model assumes:

- A massively parallel architecture with large number of main processors and specialized data processing engines (DPEs)
- ***Complexity of main processors and DPEs will remain constant, but number of processors will grow***



ITRS 2011

Figure SYSD9 SOC Consumer Stationary Design Complexity Trends

Complexity Trends for Networking SoCs

ITRS 2011 report predicts complexity trend in Networking SoCs as shown in the following chart. The model assumes:

- A multicore architecture to dominate
- Designs will include Accelerator Engines to supplement multiple cores
- ***Logic size will scale with number of cores (implying complexity of cores remains constant)***

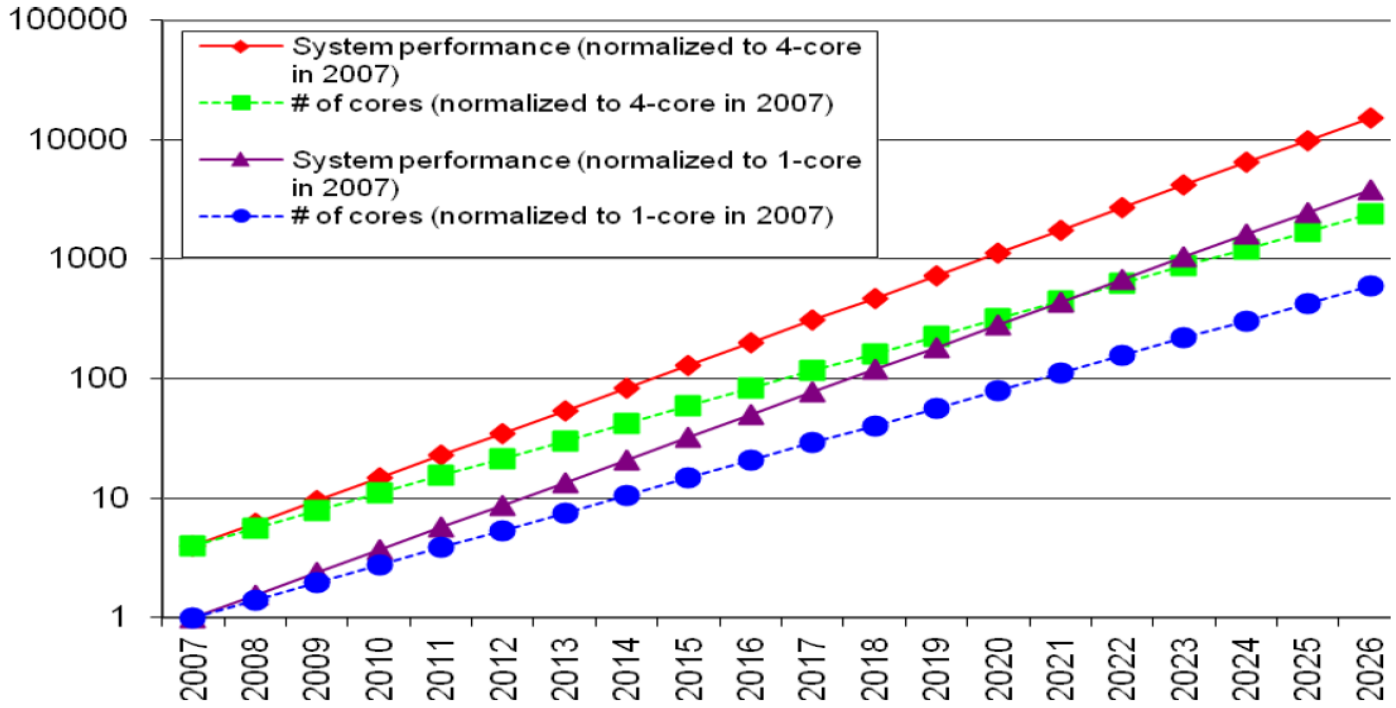
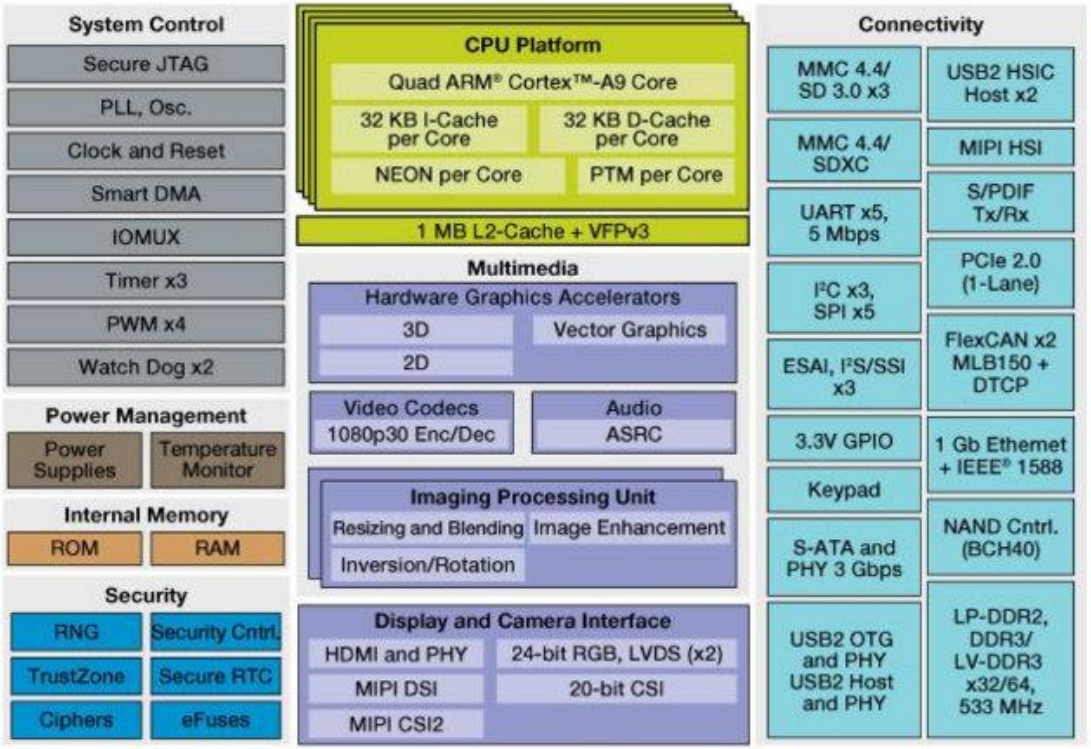


Figure SYSD2 SOC Networking Driver MC/AE Platform Performance *ITRS 2011*

More modules but not bigger ones



Freescale i.MX 6Quad SoC for Multimedia Devices

- System modules aren't getting bigger, just more numerous.
- Conclusion: Thanks to Moore's Law, FPGA capacity for logic emulation is outgrowing Rent's Rule constraints.

Experience with Big Emulation Chips

- ZeBu compiler uses high-level and low-level design structure to find the best fit.
- It naturally minimizes cut nets around major modules and sub-modules.
- We have observed that entire system modules are fitting inside ZeBu Server 3's 6.6M gate Virtex-7 FPGAs.
- Benefit to emulation speed, power, compile time.

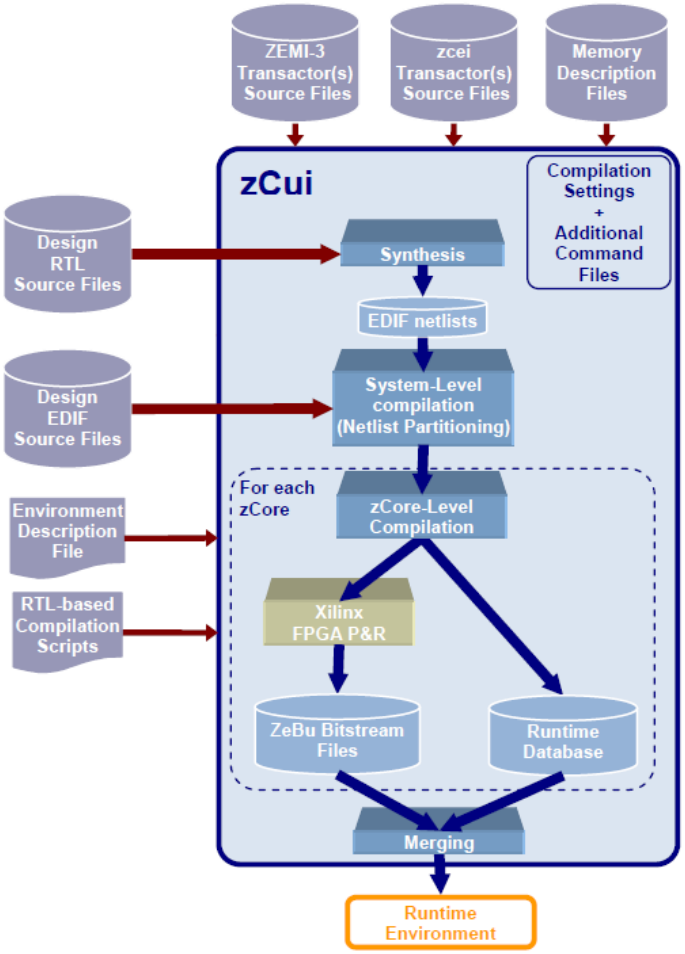


Figure 4: Compilation Flow

Moore's Law Beats Rent's Rule

1. Major system modules such as advanced 64-bit CPUs, GPUs, DSP datapaths fit inside MegaLUT FPGAs.
   – Biggest FPGA chips today, mid-range FPGAs tomorrow.
2. FPGAs will continue to follow Moore's Law as well as or better than any other form of silicon *(or beyond)*.
3. Effects of Rent's Rule on logic emulation will continue to weaken as FPGAs keep growing.

- The biggest FPGAs continue to enable the highest capacity, fastest, smallest, coolest, cheapest and most reliable logic emulators.


Thank You!